AMD

Am30LV0064D

64 Megabit (8 M x 8-Bit)
CMOS 3.0 Volt-only Flash Memory with UltraNAND™ Technology

DISTINCTIVE CHARACTERISTICS

■ **Single power supply operation**
— Full voltage range: 2.7 to 3.6 volt read, erase, and program operations
— Separate V_{CCQ} for 5 volt I/O tolerance

■ **Automated Program and Erase**
— Page program: 512 + 16 bytes
— Block erase: 8 K + 256 bytes

■ **Block architecture**
— 8 Kbyte blocks + 256 byte spare area (separately erasable, readable, and programmable)
— 512 byte page + 16 byte spare area for ECC and other system overhead information

■ **Fast read and program performance**
— Read: < 7 µs initial, < 50 ns sequential
— Program: 200 µs (full page program at 400 ns/byte)
— Erase: < 2 ms/8 Kbyte block

■ **Pinout and package**
— Industry Standard NAND compatible pinout with 8-bit I/O bus and control signals
— TSOP-II 44/40 pin package (standard and reverse) with copper lead frame for higher reliability
— 40-ball FBGA package provides higher reliability and "packing density"

■ **Command set**
— Basic Command set: Read Data, Read ID, Read Status, Input Data, Program Data, Block Erase, Erase Suspend/Resume, Reset
— Superset Command: Gapless Sequential Read Data

■ **Operation status byte**
— Provides a software method of detecting program or erase operation completion, program/erase pass/fail condition, erase suspend status, and the write protect status

■ **Operating current (typical)**
— Read: 10 mA (sequential)
— Program: 10 mA
— Erase: 10 mA
— Standby: 10 µA (CMOS)

■ **Block erase suspend/resume**
— Suspends an erase operation to read data from, or program data to, a block that is not being erased, then resumes the erase operation

■ **Ready/Busy# pin (RY/BY#)**
— Provides a hardware method of detecting program or erase cycle completion

■ **WP# input pin**
— At V_{IL}, the device is protected. Program or erase operations in the device are inhibited
— At V_{IH}, the device is unprotected. Program and erase operations are allowed

■ **Minimum 100,000 program/erase cycles guaranteed per block, without ECC (> 1 million cycles with ECC)**

■ **10-year data retention at 85°C**

GENERAL DESCRIPTION

The Am30LV0064D is a 64 Mbit mass storage Flash memory device, organized as 8 Kbyte (+256 byte) blocks (1,024 blocks total), each with 16 pages of 512 (+16) bytes (16,384 pages total).

Each device requires only a **single 3.0 volt power supply** for read, program, and erase functions. Internally generated and regulated voltages are provided for the program and erase operations. A V_{CCQ} pin is provided to allow 5 volts to be applied to the output buffer logic. With 5 volt tolerant inputs, the V_{CCQ} pin provides the Flash device with 5 volt tolerant I/O.

The Am30LV0064D is entirely command set compatible with industry standard NAND instructions and timing. Commands are written to the command register through the 8-bit I/O bus using standard NAND write timing. Register contents serve as inputs to an internal state-machine that controls the read, erase, and programming circuitry. Write cycles also internally latch addresses and data needed for the read, programming, and erase operations. Reading data out of the device is similar to reading from NAND Flash devices. The device has an initial page read access time of 7 μs, with subsequent byte accesses of less than 50 ns per byte.

Device programming occurs on a page basis by executing the Input Data and Program Data command sequences. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure is performed on a block basis and occurs by executing the Block Erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically pre-programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The **block erase architecture** allows memory blocks to be erased and reprogrammed without affecting the data contents of other blocks. The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any block that is not selected for erasure. True background erase can thus be achieved. The device is fully erased when shipped from the factory.

The host system can detect whether a sequential read, program, or Block Erase operation is complete by observing the RY/BY# pin or by reading the **status register**. After a program or erase cycle has been completed, the device is ready to accept another command.

Hardware data protection is provided by a write protect (WP#) input pin which inhibits all program and erase operations when asserted (low).

The device offers a **standby mode** as a power-saving feature. Once the system places the device into the standby mode power consumption is greatly reduced.
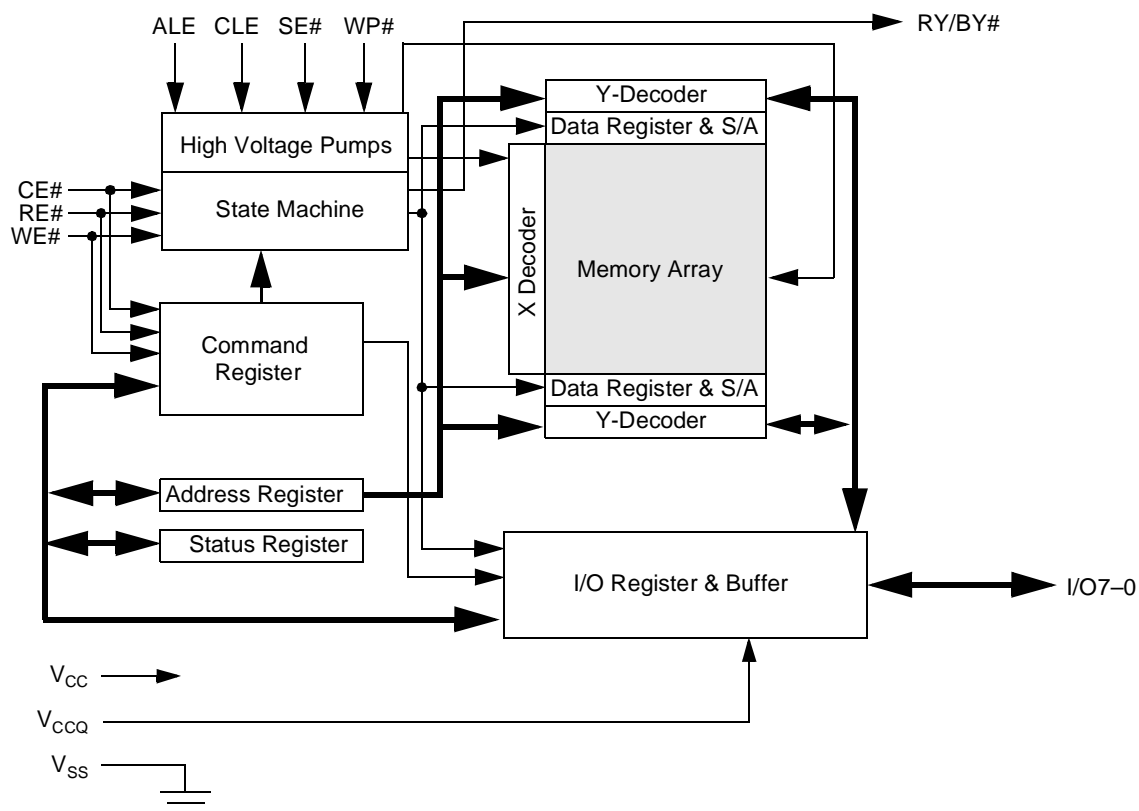
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness.

PRODUCT SELECTOR GUIDE

Family Part Number	Am30LV0064D	
Option	**J40**	**K40**
Number of Usable Blocks Guaranteed	1024	1014–1024
Percentage of Usable Blocks Guaranteed	100%	99–100%

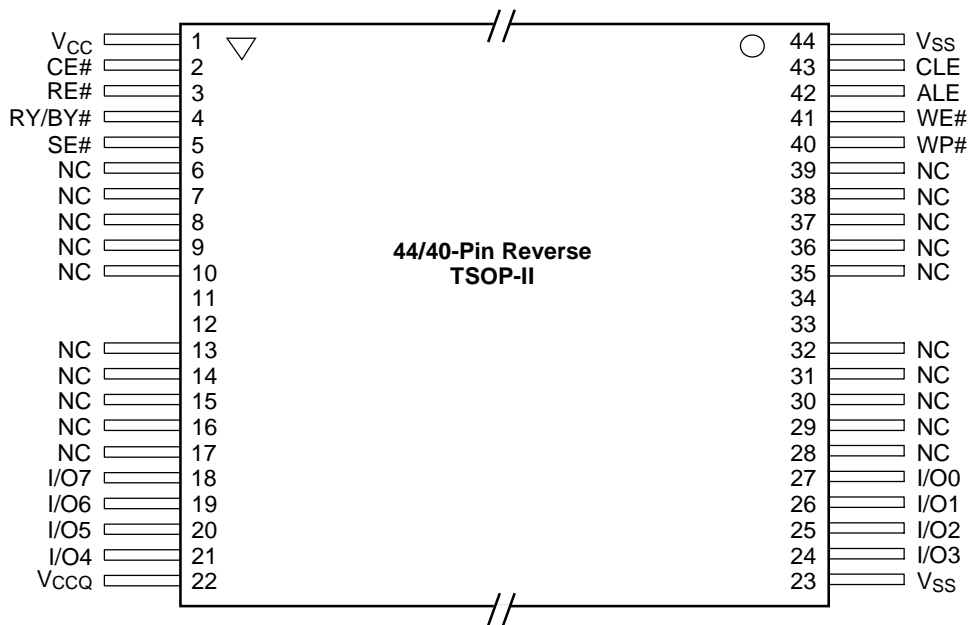*Note: See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM

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CONNECTION DIAGRAMS

		44/40-Pin Standard TSOP-II		
Vss	1 ○		44	Vcc
CLE	2		43	CE#
ALE	3		42	RE#
WE#	4		41	RY/BY#
WP#	5		40	SE#
NC	6		39	NC
NC	7		38	NC
NC	8		37	NC
NC	9		36	NC
NC	10		35	NC
	11		34	
	12		33	
NC	13		32	NC
NC	14		31	NC
NC	15		30	NC
NC	16		29	NC
NC	17		28	NC
I/O0	18		27	I/O7
I/O1	19		26	I/O6
I/O2	20		25	I/O5
I/O3	21		24	I/O4
Vss	22		23	Vccq

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		44/40-Pin Reverse TSOP-II		
Vcc	1 ▽		44 ○	Vss
CE#	2		43	CLE
RE#	3		42	ALE
RY/BY#	4		41	WE#
SE#	5		40	WP#
NC	6		39	NC
NC	7		38	NC
NC	8		37	NC
NC	9		36	NC
NC	10		35	NC
	11		34	
	12		33	
NC	13		32	NC
NC	14		31	NC
NC	15		30	NC
NC	16		29	NC
NC	17		28	NC
I/O7	18		27	I/O0
I/O6	19		26	I/O1
I/O5	20		25	I/O2
I/O4	21		24	I/O3
Vccq	22		23	Vss

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AMD ▲

CONNECTION DIAGRAMS

40-Ball FBGA
Top View, Balls Facing Down

Ø0.400 mm 0.250 SMD, Ball = 0.3 mm

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Note: *The ball grid array is depopulated to 40 signal balls. The maximum package height is 1.2 mm. The 9 x 9 x 9 x 9 outrigger balls (shaded) may be required for higher density devices in larger packages. The shaded ball region should be treated as a "keep out" area with pads placed to allow larger devices to be accommodated.*

Special Handling Instructions

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

I/O7–I/O0   = 8 Inputs/Outputs

CE#   = Chip Enable input

RE#   = Read Enable input

WE#   = Write Enable input

SE#   = Spare area Enable input

ALE   = Address Latch Enable input

CLE   = Command Latch Enable input

WP#   = Write Protect input

RY/BY#   = Ready/Busy output (open drain)

V_{CC} = 3.0 Volt-only single power supply for the Flash device core

(see Product Selector Guide for speed options and voltage supply tolerances)

V_{CCQ} = Single power supply for output buffers (see V_{CCQ} signal description)

V_{SS} = Device ground

NC   = Pin not connected internally

LOGIC SYMBOL
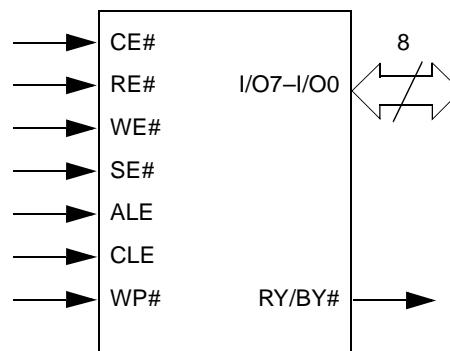
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FUNCTIONAL PIN DESCRIPTION

Input/Output Pins (I/O7–I/O0)

The eight I/O pins are used to send commands, addresses, and data to the device, and to receive data during read operations.

Command Latch Enable (CLE)

The CLE input controls activation of the command register for the receipt of commands. When CLE is high, the command is latched into the command register on the rising edge of the Write Enable (WE#) signal.

Address Latch Enable (ALE)

The ALE input controls activation of the address information during the address latch operation, or the input data during the Input Data operation. When ALE is high, the address information is latched on the rising edge of the Write Enable (WE#) signal. When ALE is low (and the CLE input is low) the Input Data information is latched on the rising edge of the Write Enable (WE#) signal.

Chip Enable (CE#)

The CE# input controls the active/standby mode during command, data, and address inputs. During the command and address latch operations, CE# must be low prior to the falling edge of Write Enable (WE#). During Input Data operations, CE# must remain low until after the rising edge of WE# during the final Data In operation. When CE# is high, and an internal operation is not in process, the device goes into standby mode and current consumption is greatly reduced.

The CE# signal is ignored during program or erase operation, as indicated by the Busy state (RY/BY# = low).

Read Enable (RE#)

The RE# input controls the serial data output and status from the I/O lines. The data output is triggered on the falling edge of RE#, with valid data available after a delay of t_{REA}. The Status output data is also triggered on the falling edge of RE#, with the status available after a delay of t_{RSTO}.

Write Enable (WE#)

The WE# input is used to control the Data/Command on the I/O lines during write operations. The I/O lines are latched on the rising edge of the WE# signal.

Write Protect (WP#)

The WP# input provides protection from inadvertent program/erase commands. The internal voltage regulator is reset when WP# is low, thereby preventing any program or erase operations from occurring.

The WP# input should be kept low (V_{IL}) during power-up until V_{CC} is above V_{CC}-min. During power-down WP# should be driven low (V_{IL}) before V_{CC} is below V_{CC}-min.

Spare Area Enable (SE#)

The SE# input controls access to the 16 bytes of spare area on each page. When SE# is not asserted (high), the spare area for the selected page is not enabled, and all input or output data is directed towards the primary 512 byte storage space. When SE# is asserted (low), access to the spare area is enabled, and data can be transferred to or from the 16 bytes of spare area for the appropriate page as needed. With SE# asserted (low) information can still be transferred to or from the 512 byte main Flash page, but when the end of the page is reached (byte 511) the device will automatically begin transferring information to or from the spare area.

During the Read Spare Area command sequence (50h) the SE# input must be asserted (low) during the command phase (CLE high). In all other cases when the spare area is to be accessed, the SE# input must be asserted (low) at least two access cycles prior to the spare area access. This would require the SE# input to be low by the time byte address 510 is selected, and SE# must remain low during the entire period that the spare area is accessed.

Ready/Busy Output (RY/BY#)

The RY/BY# output indicates the operation status of the device. When RY/BY# is high, the device is ready to accept the next operation. When RY/BY# is low, an internal program, erase, or random read operation is in progress.

RY/BY# is an open drain output pin which allows multiple RY/BY# pins to be wire-ORed together. The RY/BY# output pin requires an external pull-up resistor to V_{CC} (or V_{CCQ}) for proper operation.

Device Power Supply (V_{CC})

The minimum V_{CC} operating voltage for the Am30LV0064D is 2.7 volts. The device has an operating voltage range from 2.7 volts to 3.6 volts.
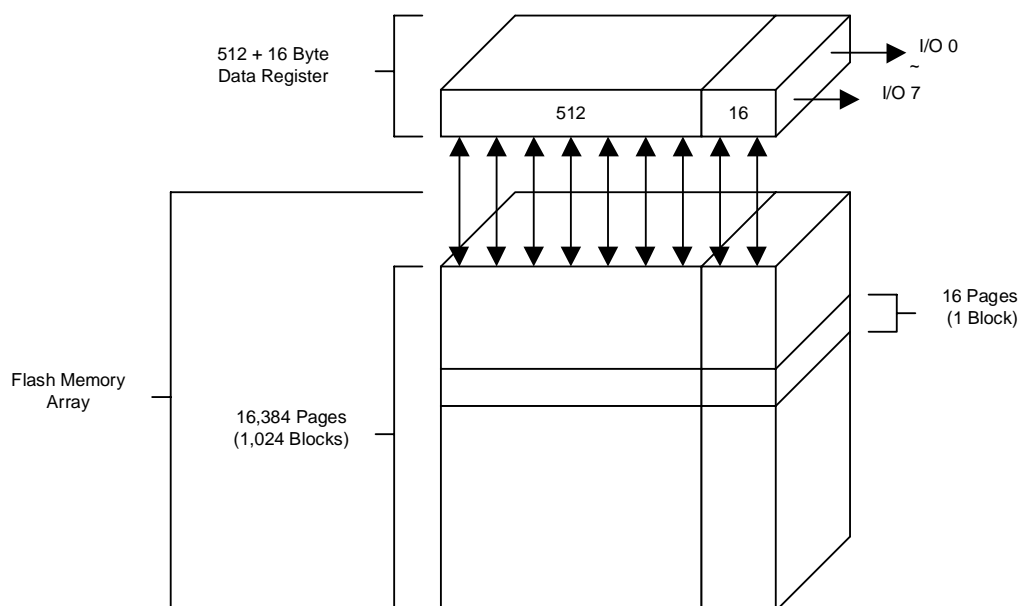
Output Buffer Power Supply (V_{CCQ})

The output voltage generated on the device is determined based on the V_{CCQ} power supply input level. A V_{CCQ} of 2.7 to 3.6 volts will allow the device to function as a 3.0 Volt-only device. A V_{CCQ} of 4.5 to 5.5 volts provides 5 volt I/O tolerance.

All input only signals are 5 volt tolerant by design, independent of the voltage on V_{CCQ}.

Ground (V_{SS})

The V_{SS} pins on the device must be grounded.

CELL LAYOUT AND ADDRESS ASSIGNMENT

512 + 16 Byte
Data Register

512   16

I/O 0
~
I/O 7

16 Pages
(1 Block)

Flash Memory
Array

16,384 Pages
(1,024 Blocks)

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Note: Device programming is executed on a page basis while erase is performed on a block basis. During read operations, data is transferred from the Flash array to the internal Data Register on a page basis. Data is then sequentially read from the Data Register on a Byte basis.

Figure 1.   Mass Storage Device Cell Layout

Table 1.   Address Assignment

	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
First Cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second Cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third Cycle	X	X	A22	A21	A20	A19	A18	A17

Legend:

Axx = specific address bit, X = don't care (V_{IH} or V_{IL})

Notes:

1. *A8 is automatically set "Low" or "High" by the 00h or 01h command.*

2. *A22 to A13 specifies the Block Address, A12 to A9 specifies the Page Address within a block, and A7 to A0 identifies the byte address within a page.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The Ordering Part Number or OPN (Valid Combination) is formed by a combination of the elements below.

Am30LV0064D   J40   E2   C   T

PACKING METHOD

T = Tape and Reel

TEMPERATURE RANGE

C = Commercial (0°C to +70°C)

I = Industrial (–40°C to +85°C)

E = Extended (–55°C to +125°C)

PACKAGE TYPE

E2   =   44/40-Pin Thin Small Outline Package (TSOP-II) Standard Pinout

F2   =   44/40-Pin Thin Small Outline Package (TSOP-II) Reverse Pinout

TBD   =   40-Ball Fine Pitch Ball Grid Array (FBGA) 0.80 mm pitch, 8 x 15 mm package

PERFORMANCE RANGE

J40 = 1024 (100%) usable sectors
K40 = 1014–1024 (99–100%) usable sectors

DEVICE NUMBER/DESCRIPTION

Am30LV0064D
64 Megabit (8 M x 8-Bit) CMOS 3.0 Volt Flash Memory with UltraNAND™ Technology
2.7–3.6 Volt with 5 Volt I/O Tolerance

Valid Combinations	
Am30LV0064DJ40	E2C, E2I, E2E,
	F2C, F2I, F2E,
Am30LV0064DK40	TBDC, TBDI, TBDE

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS, COMMAND SET, AND COMMAND DEFINITIONS

This section describes the requirements and use of the device bus operations, the command set, and the command definitions. The device bus operations are initiated through the internal command register which decodes the command to determine the current operation to be performed. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine whose outputs dictate the function of the device. Table 2 lists the device bus operations including the inputs and control levels they require, and the resulting output. Table 3 lists the command set, and Table 4 lists the command definitions. The "Device Operations" section describes each of these operations in detail.

Table 2.   Am30LV0064D Device Bus Operations

Operation	CE#	RE#	WE#	SE#	CLE	ALE	WP#	I/O7–I/O0
Read Data Area	L	L	H	L/H	L	L	X	D_{OUT}
Read Spare Area	L	L	H	L	L	L	X	D_{OUT}
Read ID, Status	L	L	H	X	L	L	X	D_{OUT}
Write Data	L	H	L	L/H	L	L	X	D_{IN}
Write Command	L	H	L	X	H	L	X	C_{IN}
Write Address	L	H	L	X	L	H	X	A_{IN}
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V $V_{SS} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V $V_{SS} \pm 0.3$ V	High-Z
Write Protect	X	X	X	X	X	X	(See Note)	X

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, X = Don't Care, A_{IN} = Address In, C_{IN} = Command In, D_{IN} = Data In, D_{OUT} = Data Out

Note: *If WP# = V_{IL}, the Flash device is protected and will not allow program or erase operations to occur. If WP# = V_{IH}, the device is unprotected and may be programmed or erased.*

Table 3.   Am30LV0064D Command Set

Operation	Cycle 1	Cycle 2	Valid During Busy
Read Data	00h/01h	–	No
Gapless Read	02h	–	No
Read Spare Area	50h	–	No
Read ID	90h	–	No
Read Status	70h	–	Yes
Input Data	80h	–	No
Page Program	10h	–	No
Block Erase	60h	D0h	No
Erase Suspend	B0h	–	Yes
Erase Resume	D0h	–	No
Reset	FFh	–	Yes

Table 4.   Am30LV0064D Command Definitions

Command Sequence (Note 2)	Bus Cycles (Note 1)											
	First		Second		Third		Fourth		Fifth		Sixth	
	Oper.	Data	Oper.	Data	Oper.	Data	Oper.	Data	Oper.	Data	Oper.	Data
Read Data Area–First Half Page	WR	00	WR	SA	WR	SA	WR	SA	RD	Data	Etc.	Etc.
Read Data Area–Second Half Page	WR	01	WR	SA	WR	SA	WR	SA	RD	Data	Etc.	Etc.
Read Data Area–Gapless Read (Note 3)	WR	02	WR	SA	WR	SA	WR	SA	RD	Data	Etc.	Etc.
Read Spare Area (Note 4)	WR	50	WR	SA	WR	SA	WR	SA	RD	Data	Etc.	Etc.
Read ID	WR	90	WR	00	RD	01	RD	E6				
Read Status	WR	70	RD	SR	Etc.	Etc.						
Input Data	WR	80	WR	SA	WR	SA	WR	SA	WR	Data	Etc.	Etc.
Program Data	WR	10										
Block Erase (Note 5)	WR	60	WR	BA	WR	BA	WR	D0				
Erase Suspend (Note 6)	WR	B0										
Erase Resume (Note 7)	WR	D0										
Reset	WR	FF										

Legend:

WR = Write Cycle, RD = Read Cycle, SA = Starting Address, Etc. = previous sequence continues as needed,
SR = Status Register, AR = Address Register, DR = Data Register, BA = Block Address

Notes:

1. All values are in hexadecimal.

2. See Table 2 for description of bus operations.

3. The Gapless Read command is similar to the Read Data Area commands except that the 7 µs latency does not occur when the Page address pointer steps to the next page to be read. This command requires that the starting byte address is located within the first half of the selected Page.

4. For the Read Spare Area command it is necessary for the SE# pin to be low during the CLE cycle and when actively reading from the 16 byte Spare Area. For all other commands the SE# pin must be low at least two cycles

prior to the first spare area access at byte address 512 (low before byte address 510).

5. The two byte Block Address cycles load address bits A22–A9 into the device. Since only address bits A22–A13 are required for a Block address, address bits A12–A9 are don't care.

6. The system may read and program in non-erasing Blocks when in the Erase Suspend mode. The Erase Suspend command is valid only during a Block erase operation.

7. The Erase Resume command is valid only during the Erase Suspend mode.

DEVICE OPERATIONS

When the AMD Mass Storage Flash device powers up, the command decoder is initialized with the Read Data command active and set to start in the first half page (op-code 00h). In order to perform any other function, the device must be programmed for the desired operation. Specific commands must be issued to the device to select one of the read modes, to input or program data, to perform one of the block erase functions, or to reset the device.

There are a number of commands available for reading information from the Mass Storage Flash device. These include Read Data to read out of the Flash array, Gapless Read to read data in a special high performance mode, Read Spare Area to read the 16 byte spare area in each page, Read ID to determine the manufacturer and device ID, and Read Status to check the device status.

Programming data into the Flash array is a two step process and requires that two separate command sequences be performed. The data to be programmed must first be loaded into the Data Registers using the Input Data command sequence. After the data is loaded the Page Program command is performed to transfer the information from the Data Registers to the Flash array.

Device erasure occurs on an 8 Kbyte block basis, with each block in the device containing 16 pages and the respective spare area for each page. During block erase, the Flash device supports erase suspend and erase resume to allow time critical tasks to be performed during erase. These time critical tasks can be to read or program in a block that is not currently selected for erasure.

The Flash device also supports a reset command sequence to reset the device and return it to the Read Data command state.

All of the commands and their functions supported by the Flash device are described in the following sub-sections with simplified timing diagrams included. The timing diagrams are intended to illustrate the relationship of each of the control, status, and data signals for each of the command sequences. Please refer to the AC/DC Characteristics section for more complete timing information.

In each of the simplified timing diagrams, the polling period during device busy (RY/BY# = V_{IL}) is not shown. During device busy the system can poll the device internal status register or monitor the RY/BY# pin to determine when the internal operation is complete.

Read Operations

Read Data (00h / 01h)

There are two commands available for reading from the Flash array (via the Data Registers). These are the Read Data starting with the first half page (00h) and Read Data starting with the second half page (01h).

The commands are identical except for the starting region within the selected page. After the command cycle, three address cycles are used to input the starting address for the read operation. Upon the rising edge of the final WE# pulse there is a 7 µs latency in which 528 bytes of information are transferred from the Flash array page to the 528 byte Data Register. During the 7 µs latency period the Flash device will appear busy and the RY/BY# signal or the status register may be used to monitor the completion of the data transfer. Only the Reset and Read Status commands are valid during the period that the device is busy. Once the information has been loaded into the Data Register, it

may be sequentially read with consecutive 50 ns RE# pulses. Each RE# pulse will automatically advance the column address by one. Once the last column has been read, the page address will automatically increment by one and the Data Register will be updated with information from the new page after a 7 µs latency period.

During the sequential read mode, if the Spare Area Enable input (SE#) is high, the column address will advance to address 511 and then the page address will increment by one. If the SE# input is low, the column address will advance to address 527 before the page address is incremented. This allows the information in the Spare Area to be read at the end of the page before the next page of information is transferred into the Data Registers. In the case of the Read Data command, the SE# input may go low anytime from before the command is issued to before address 510 is accessed. This allows the Flash internal logic to correctly enable the Spare Area for reading.
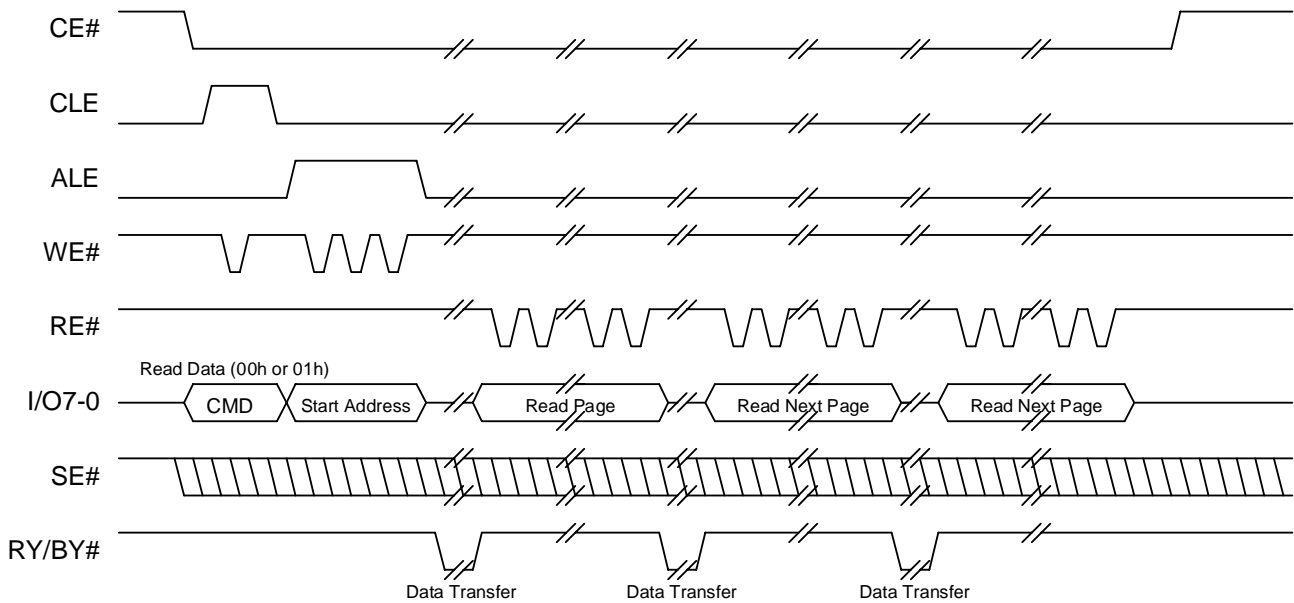
22203A-7

Figure 2.   Read Data

Gapless Read (02h)

The Gapless Read command is almost identical to the Read Data command, except that it allows reading from multiple pages with only one 7 µs latency occurring on the first page transfer. After the command cycle is used to write the Gapless Read op-code to the device, three address cycles are used to input the starting address for the Gapless Read operation.

The Gapless Read operation requires that the address entered specifies an address location in the first half of the selected page. Upon the rising edge of the final WE# pulse there is a 7 µs latency in which 528 bytes of information are transferred from the Flash array page to the 528 byte Data Register. During this 7 µs period the device will appear busy and the RY/BY# signal or the status register may be used to monitor the completion of the data transfer. Only the Reset and Read Status commands are valid during the period that the device is busy. Once the information has been loaded into the Data Register, it may be sequentially read with consecutive 50 ns RE# pulses. Each RE# pulse will automatically advance the column address by one. Once the last column has been read, the page address will automatically increment by one and the Data Register will be updated with the new page.

In the case of the Gapless Read, there is no 7 µs latency period encountered when moving from the current page to the next sequential page.

During the sequential read mode, if the Spare Area Enable input (SE#) is high, the column address will advance to address 511 and then the page address will increment by one. If the SE# input is low, the column address will advance to address 527 before the page address is incremented. This allows the information in the Spare Area to be read at the end of the page before the next page of information is transferred into the Data Registers.

This is an AMD superset command which is not available on competitive devices in the marketplace.
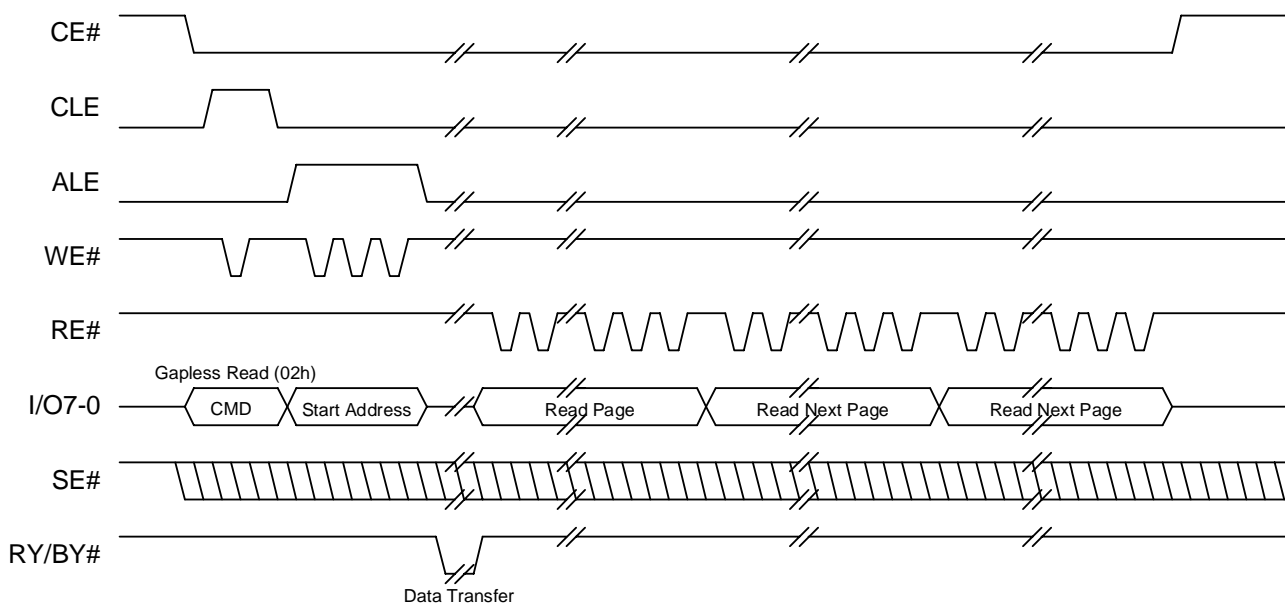
22203A-8

Figure 3.   Gapless Read

Read Spare Area (50h)

The Read Spare Area command is similar to the Read Data command, except that it only reads information from the selected page 16 byte Spare Area (address locations 512 through 527). After the command cycle is used to write the Read Spare Area op-code to the device, three address cycles are used to input the starting address for the read operation. During the Read Spare Area command cycle the SE# input must be low.

Because the Read Spare Area operation only reads the 16 byte spare area in the page, address bits A7–A4 are don't care. Address bits A22–A9 are used to select the Page, and address bits A3–A0 are used to select the starting byte within the Spare Area of the Page. Upon the rising edge of the final WE# pulse there is a 7 µs latency in which all 528 bytes of information are transferred from the Flash array page to the 528 byte Data Register. Following the data transfer the internal address pointer will point to the byte selected in the Spare Area. During the 7 µs data transfer period the device will appear busy and the RY/BY# signal or the status register may be used to monitor the completion of the data transfer. Only the Reset and Read Status commands are valid during the period that the device is busy. Once the information has been loaded into the Data Register, the Spare Area information may be sequentially read with consecutive 50 ns RE# pulses. Each RE# pulse will automatically advance the Spare Area column address by one. Once the last column has been read, the page address will automatically increment by one and the Data Register will be updated with the new page after a 7 µs latency.

During the sequential read mode, the Spare Area Enable input (SE#) must be low. This is necessary any time the Spare Area is being read. In this operation, the column address will advance from the selected starting byte location to address 527 before the page address is incremented. After the next page of information is transferred to the Data Register, sequential read operations will begin in the Data Register at address location 512. Unlike the Read Data and Gapless Read modes, the Read Spare Area operation requires that the SE# input be asserted low prior to the command being issued to the device.
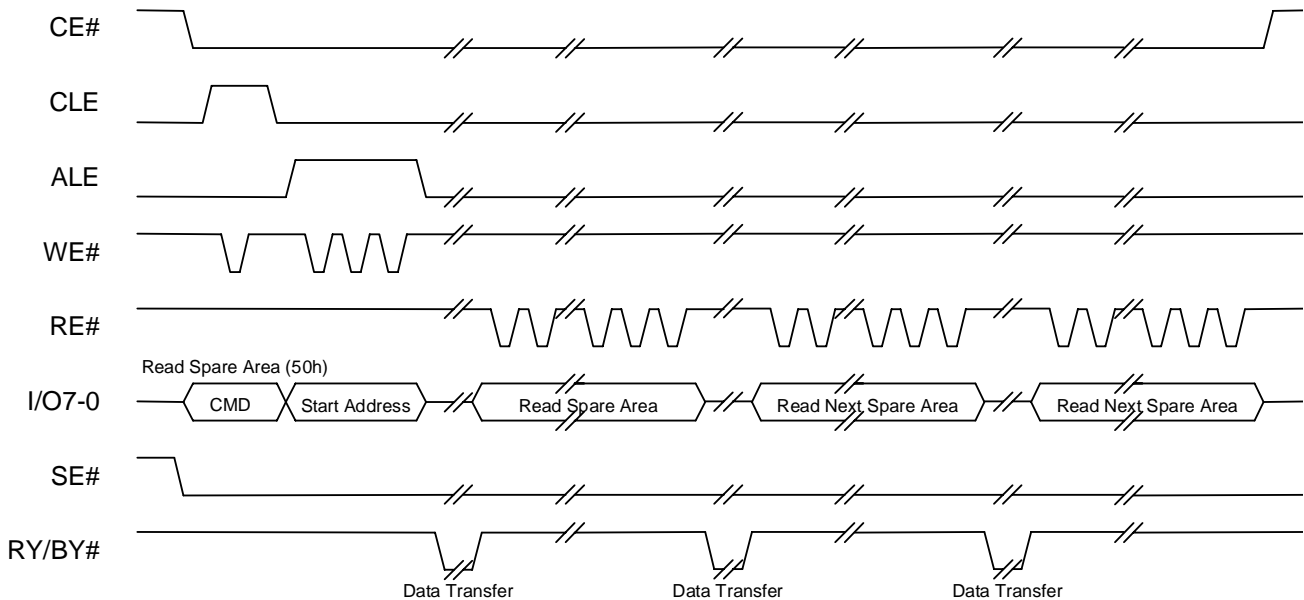
22203A-9

Figure 4.   Read Spare Area

Read ID (90h)

The Read ID operation is used to read the Manufacturers ID and the Device ID from the Flash device. After the command cycle, one address cycle is used to input a 00h value into the device. Upon the rising edge of the final WE# pulse, the two bytes of information may be sequentially read with two consecutive 50 ns RE# pulses.

Table 5.   Am30LV0064D ID Codes

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	ID Code
Manufacturer	0	0	0	0	0	0	0	1	01h
Device	1	1	1	0	0	1	1	0	E6h
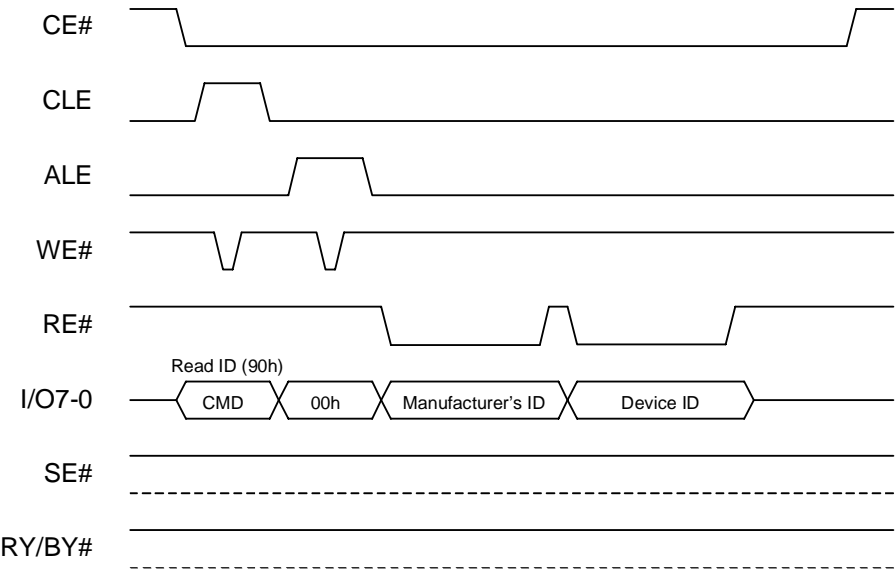
22203A-10

Figure 5.   Read ID

Read Status (70h)

The Read Status operation is used to read the device status to determine if the device is ready, in the write protect mode, erase suspended, or if the previous program/erase operation completed without error. After the rising edge of the command cycle WE# pulse, the falling edge of CE# or RE#, whichever occurs last, will output the contents of the status register on the 8 I/O pins, I/O7–I/O0. The status register is constantly updated and does not require either CE# or RE# to be toggled. By utilizing the Read Status operation, multiple devices with RY/BY# pins wired together may be polled to determine their specific status.
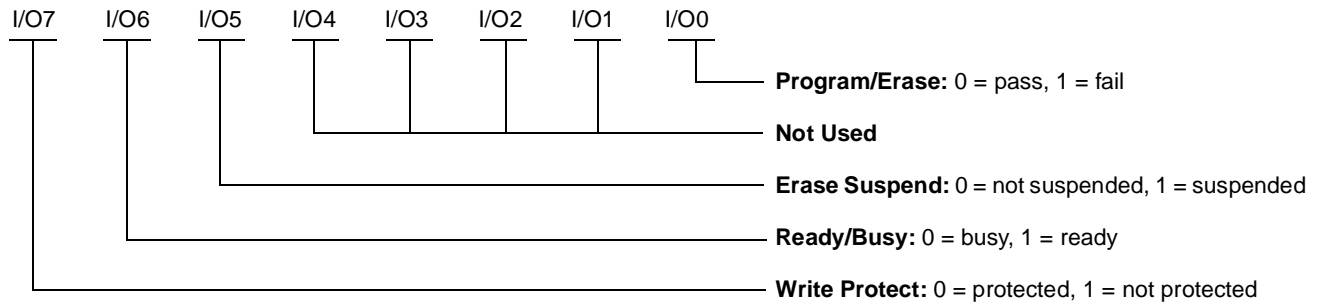
22203A-11

Figure 6.   Device Status Register Bit Definition
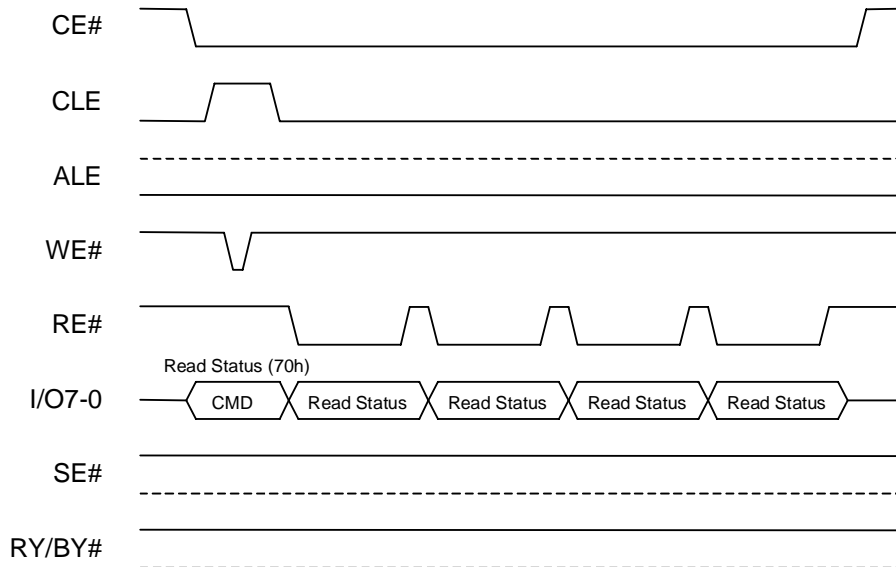
22203A-12

Figure 7.   Read Status

Program Operations

Input Data (80h)

The Input Data command sequence is the first of two operations that must be performed to program information into one of the Flash pages. The second operation, Page Program, is used to transfer information from the Data Registers to the Flash array after the Input Data procedure loads the Data Registers. In order to set the starting region within the Data Registers (first half, second half, or Spare Area), the appropriate command (00h, 01h, 50h) should be issued prior to the Input Data command being performed. If a command is not submitted to assign the starting region, the starting region will be determined by its previous state.

After the command cycle, three address cycles are used to input the starting address for the Input Data operation. Upon the rising edge of the final WE# pulse, between 1 and 528 bytes of information can be loaded into the Data Register with consecutive 50 ns WE# pulses. Each WE# pulse will automatically advance the Data Register address pointer by one. If additional write pulses are issued after the last address has been written (511 if SE# is high or 527 if SE# is low), the Data Register address pointer will wrap around to 0. If additional WE# pulses are issued, the device will continue to store information into the Data Register until a new command is issued.

The Spare Area Enable input (SE#) must be low by the time address 510 is accessed in order to load information into the last 16 bytes of the Data Register. If the SE# input is high, the Data Register address will advance to address 511. If the SE# input is low, the column address will advance to address 527. This allows information that needs to be programmed into the Spare Area of the page to be loaded into the Data Registers properly. Please refer to Figure 8 for the simplified timing diagram for Input Data and Page Program.

Page Program (10h)

The Page Program command sequence is issued after the Input Data operation has loaded the proper data in the Data Registers. Upon the rising edge of the command cycle WE# pulse, this operation transfers information from the Data Registers to the Flash array in 200 μs or less, and the Flash device will appear busy during the data transfer operation. The RY/BY# signal or the status register may be used to monitor completion of the data transfer. Only the Reset and Read Status commands are valid during the period that the device is busy.

Only those bytes loaded with the Input Data command sequence will be programmed in the Flash array. This allows partial page programming to be performed as needed. If no bytes were loaded into the Data Register, or if the Page Program command is issued without the Input Data command being performed, no program operation will occur. A given page may not be partially programmed more than 10 consecutive times without an intervening erase operation being performed on the page. After programming a page, the status register bit I/O0 should be checked to verify that the program operation completed properly.

The Spare Area Enable input (SE#) must be low in order to program information into the last 16 bytes of the page that is selected for programming. If the SE# input is high, the Spare Area will not be programmed.

Please refer to Figure 8 for the simplified timing diagram for Input Data and Page Program and to Figure 9 for a flow chart describing the device program procedure.
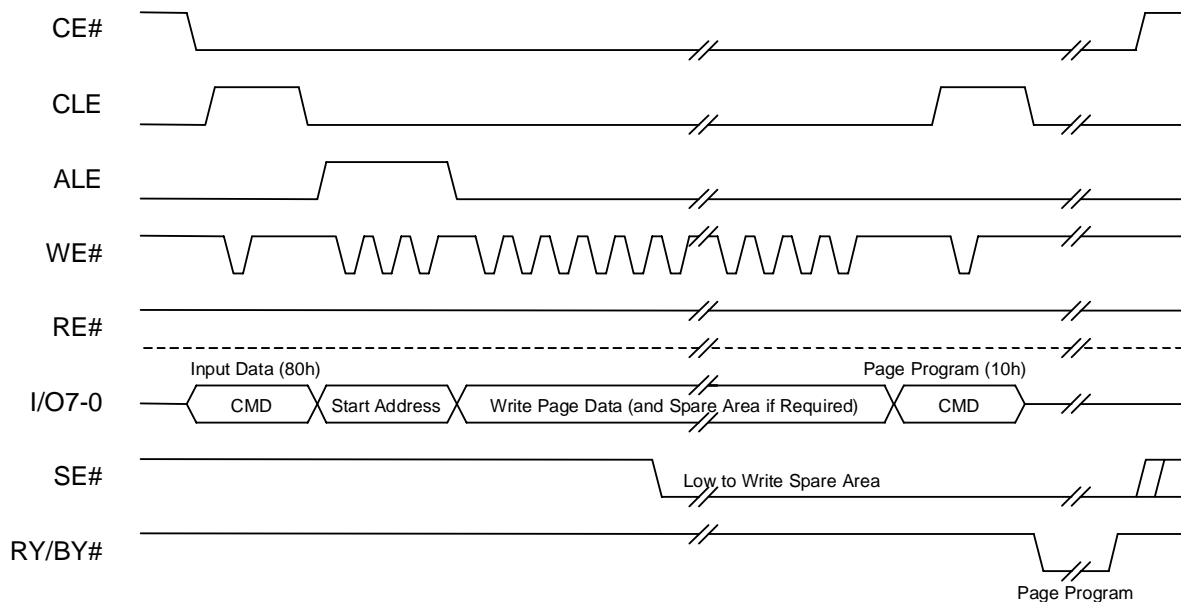
22203A-13

Figure 8.   Input Data and Page Program
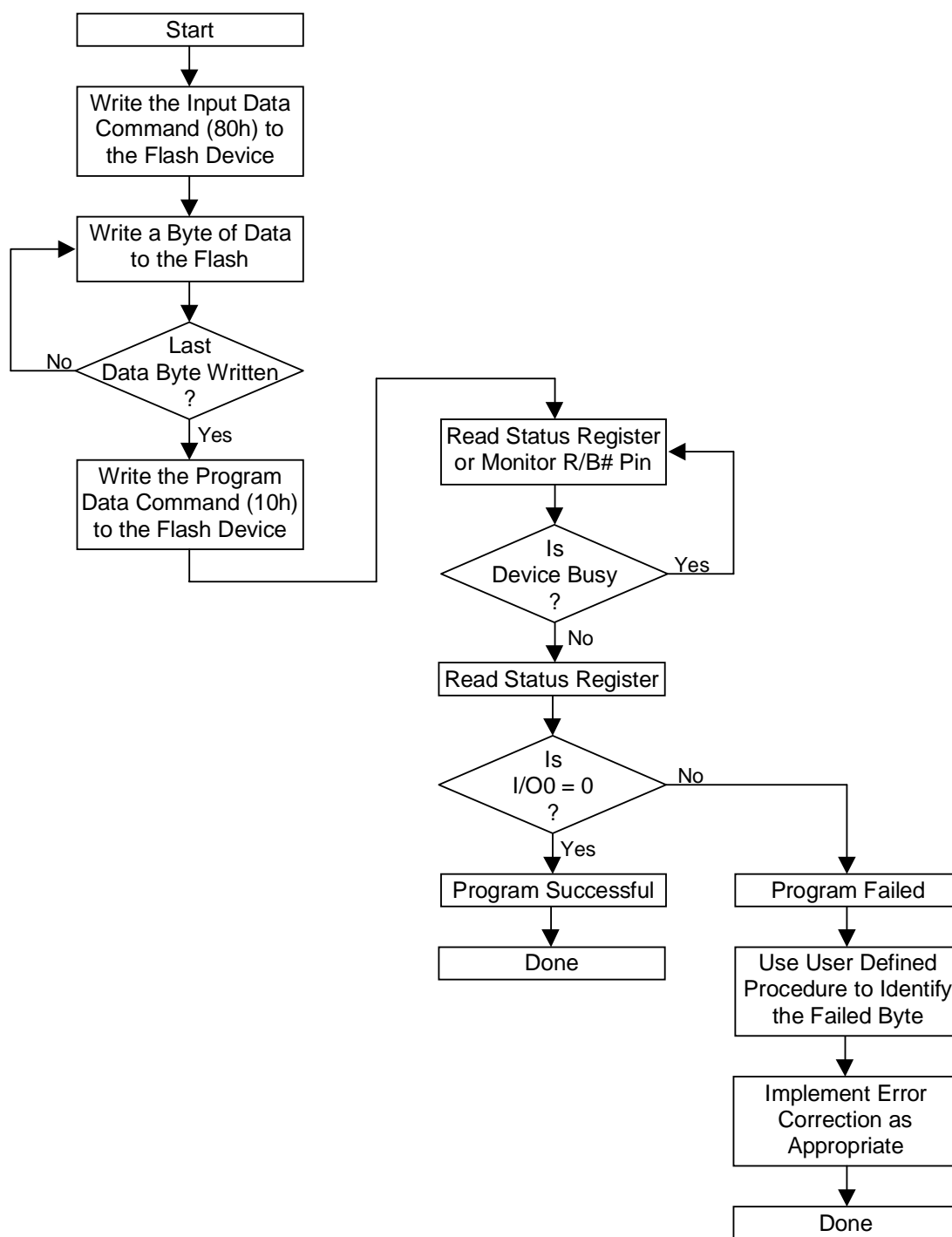
Figure 9.   Program Operations Flow Chart

Erase Operations

Block Erase (60h) (D0h)

The Block Erase command sequence is a two command operation procedure that must be performed to erase information in one of the 16 page Flash blocks.

After the first command cycle, two address cycles are used to input the block address for the block to be erased. Since the block address only requires address bits A22–A13 to determine the block address, bits A12–A9 are don't care. After the two address cycles are complete, the second command cycle is issued.

Upon the rising edge of the final WE# pulse for the second command cycle, the Flash device will begin the Block Erase operation.

A block will typically erase in the Flash array in 2 ms or less and is guaranteed to erase within 10 ms. The Flash device will appear busy during the Block Erase operation and the RY/BY# signal or the status register may be used to monitor completion of the erase. Only the Erase Suspend, Reset, and Read Status commands are valid during the period that the device is busy.

After erasing a block, the status register bit I/O0 should be checked to verify that the erase operation completed properly. Figure 10 shows the simplified timing for Block Erase.
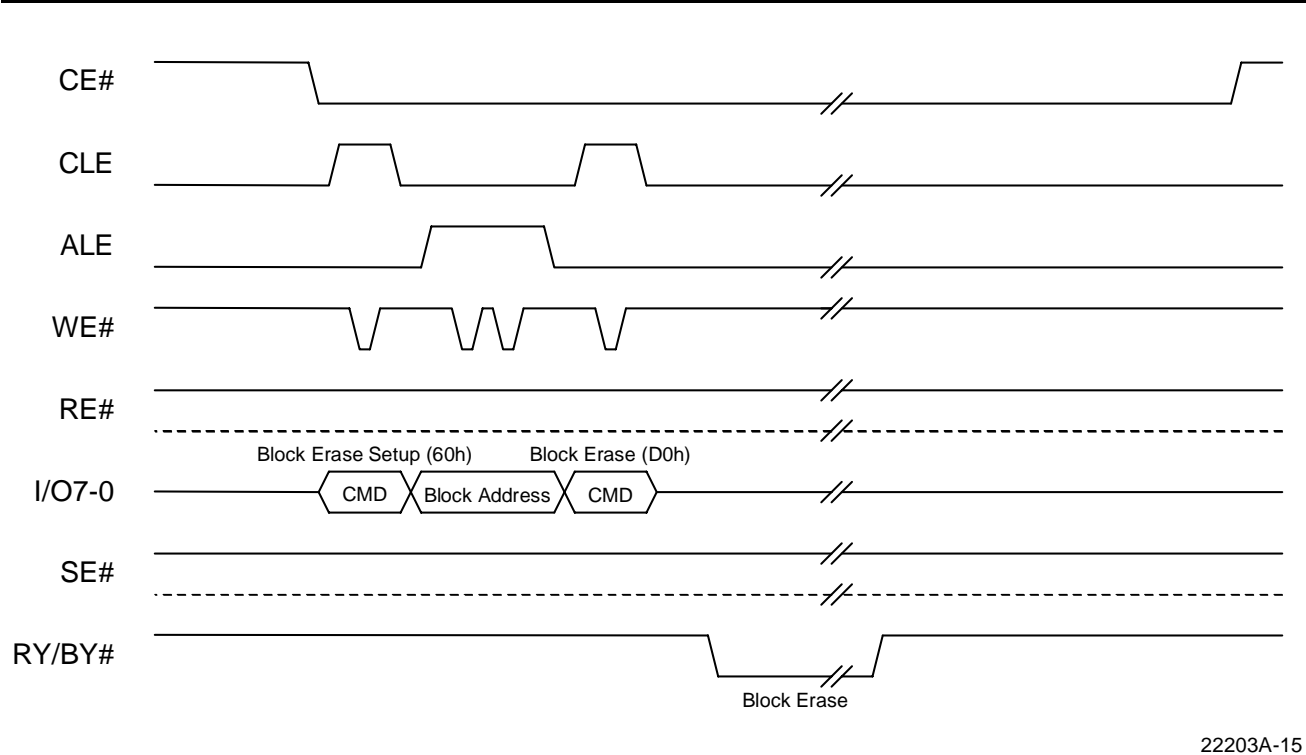
22203A-15

Figure 10. Block Erase

Erase Suspend (B0h)

The Erase Suspend command sequence is only valid during a Block Erase operation. Upon the rising edge of the command WE# pulse, the Flash device will suspend the Block Erase operation. The RY/BY# signal or the status register may be used to determine when the Block Erase has actually been suspended. Once the Erase Suspend has taken effect, read or program operations may be performed in blocks that are not selected for erasure.

Once a Block Erase has been suspended, the suspended Block Erase operation must be completed before another block can be selected for erasure. When the Erase Suspend command is issued, the Block Erase command is inhibited. The Block Erase will be invalid until an Erase Resume command allows the suspended erase to complete, the device is reset, or power is removed from the device. Refer to Figure 11 for a simplified timing diagram showing the sequence

of events required to implement Erase Suspend during a block erase operation.

Erase Resume (D0h)

The Erase Resume command sequence is only valid during an Erase Suspend operation. Upon the rising edge of the command WE# pulse, the Flash device will resume the Block Erase operation that was suspended. The RY/BY# signal or the status register may be used to determine when the Block Erase completes.

After the block finishes the erase operation, the status register bit I/O0 should be checked to verify that the erase completed properly. Refer to Figure 11 for a simplified timing diagram describing how to execute an Erase Resume operation during Erase Suspend to allow the previously suspended block erase to complete.
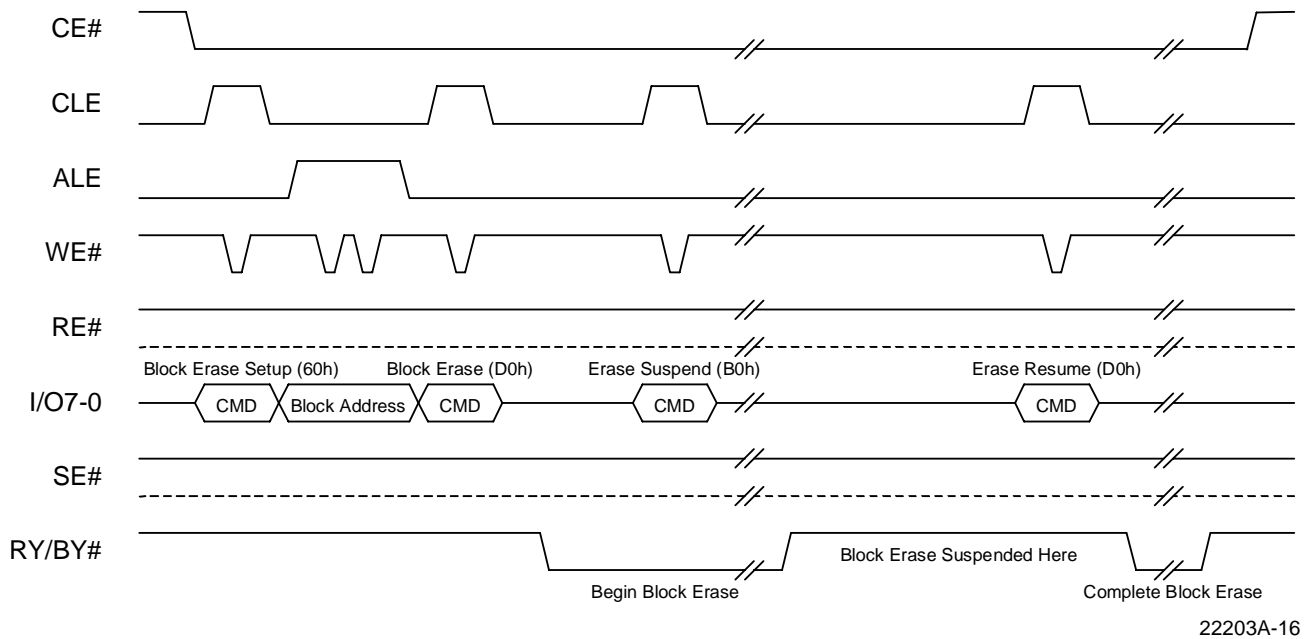
Figure 11.   Erase Suspend and Erase Resume

22203A-16

Reset Operation

Reset (FFh)

The Reset command sequence can be issued any time the Flash device needs to be initialized. This may be required when the device is busy during program, erase, or data transfer operations. Reset will take place on the rising edge of the command cycle WE# pulse. If the WP# input is high, not protected, the Status Register will be set to C0h.

If a second Reset command is issued while a reset is in process, the second Reset command will be ignored. If a Reset command is issued during a program or erase operation, the internal high voltages will be discharged before the device indicates that it is ready (reset complete).

The RY/BY# signal or the status register may be used to determine when the Reset operation is done. Figure 12 shows a simplified timing diagram of the reset command sequence.

22203A-17
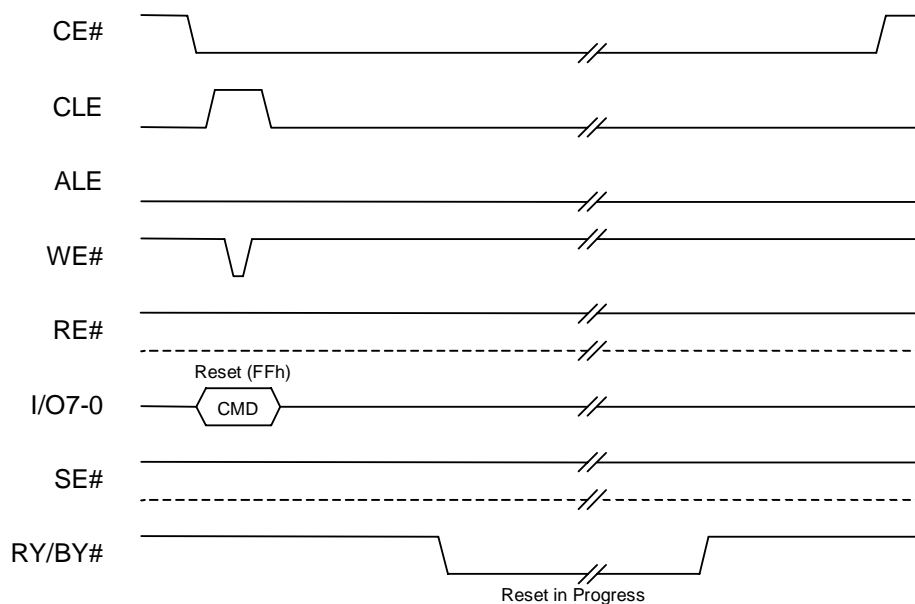
Figure 12.   Reset

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . –0.5 V to +4.0 V

V_{CCQ} (Note 2) . . . . –0.5 V to +6.0 V

All other pins (Note 1) . . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 13. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 14.*

2. *For 3.0 volt-only applications, V_{CCQ} should be connected to V_{CC}. To provide 5 V tolerant I/O, V_{CCQ} should be between 4.5 and 5.5 V.*

3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . .–40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . .–55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . . . 3.0 V to 3.6 V

V_{CC} for full voltage range. . . . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.
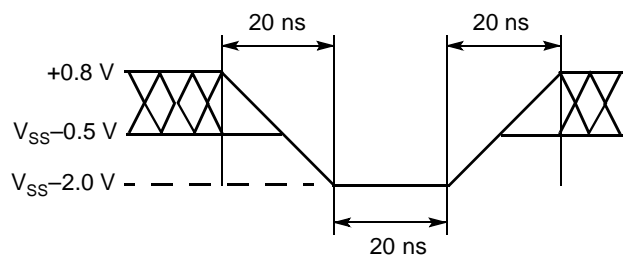
22203-18

Figure 13. Maximum Negative Overshoot Waveform
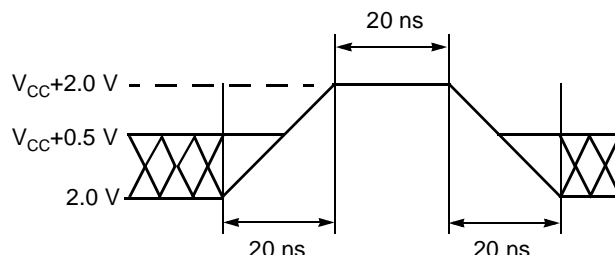
22203-19

Figure 14. Maximum Positive Overshoot Waveform

AMD

DC CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{CC1}	Sequential Read Current	t_{CYCLE}=50 ns, CE#=V_{IL}, I_{OUT}=0 mA	–	10	20	mA
I_{CC2}	Command, Address Input Current	t_{CYCLE}=50 ns, CE#=V_{IL}	–	10	20	mA
I_{CC3}	Data Input Current	–	–	10	20	mA
I_{CC4}	Program Current	–	–	10	20	mA
I_{CC5}	Erase Current	–	–	10	20	mA
I_{SB1}	Standby Current (TTL)	CE#=V_{IH}	–	–	1	mA
I_{SB2}	Standby Current (CMOS)	CE#=V_{CC}–0.2 V, WP#= SE# = 0V/V_{CC}, RESET# = 0V/V_{CC}	–	10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	–	–	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to 3.6 V	–	–	10	µA
V_{IH}	Input High Voltage	All I/O Pins	2.0	–	V_{CCQ} + 0.3	V
		All Except I/O Pins	2.0	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage, All Inputs	–	–0.3	–	0.8	V
V_{OH}	Output High Voltage	I_{OH}= –400 µA	V_{CC} – 0.3	–	–	V
V_{OL}	Output Low Voltage	I_{OL}=2.1 mA	–	–	0.4	V
I_{OL} (RY/BY#)	Output Low Current (RY/BY#)	V_{OL}=0.4 V	8	10	–	mA

AC CHARACTERISTICS

Command, Data, and Address Input

Parameter		Description	Min	Max	Unit
JEDEC	Std.				
	t_{ALS}	ALE Setup Time	0	–	ns
	t_{ALH}	ALE Hold Time	10	–	ns
	t_{CLS}	CLE Setup Time	0	–	ns
	t_{CLH}	CLE Hold Time	10	–	ns
	t_{CES}	CE# Setup Time	0	–	ns
	t_{CEH}	CE# Hold Time	10	–	ns
	t_{DS}	Data Setup Time	20	–	ns
	t_{DH}	Data Hold Time	10	–	ns
	t_{WC}	Write Cycle Time	50	–	ns
	t_{WP}	WE# Pulse Width	25	–	ns
	t_{WH}	WE# Pulse Width High	15	–	ns

Normal Operation

Parameter		Description	Min	Max	Unit
JEDEC	Std.				
	t_{ALRE}	ALE to RE# Delay for Data Read	50	–	ns
	t_{AR}	ALE to RE# Delay for ID and Manufacturer Read	100	–	ns
	t_{CEH}	CE# Pulse Width High	100	–	ns
	t_{CELS}	CE# Low to Status Output Valid	–	45	ns
	t_{CHZ}	CE# High to Output High Impedance	–	20	ns
	t_{CR}	CE# Low to RE# Low	100	–	ns
	t_{CRY}	CE# High to RY/BY# High	–	50 + t (See Note)	ns
	t_{RC}	Read Cycle Time	50	–	ns
	t_{RP}	RE# Pulse Width	35	–	ns
	t_{REH}	RE# Pulse Width High	15	–	ns
	t_{REA}	RE# Access Time for Data Read	–	35	ns
	t_{REA2}	RE# Access Time for ID and Manufacturer Read	–	35	ns
	t_{RHZ}	RE# High to Output High Impedance	15	30	ns
	t_{RLS}	RE# Low to Status Output Valid	–	35	ns
	t_{WHR}	WE# High to RE# Low	60	–	ns
	t_{OZR}	Output High Impedance to RE# Low	0	–	ns
	t_{RB}	Last RE# Rising Edge to RY/BY# Low	–	100	ns
	t_{RR}	RY/BY# High to RE# Low	20	–	ns
	t_{WB}	WE# High to RY/BY# Low	–	100	ns
	t_{R}	Transfer Time from Flash Array to Data Register	–	7	µs
	t_{RST}	Reset Time (Read/Program/Erase/after Erase Suspend)	–	5/10/500/5	µs
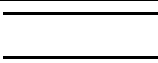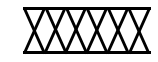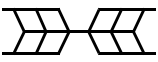
Note: Time is dependent on value of pull-up resistor at RY/BY# pin.

AMD⏗

AC CHARACTERISTICS
Mode Selection

ALE	CLE	WE#	CE#	RE#	SE#	WP#	RY/BY#	Mode
L	H	⎍↑	L	H	X	X	H	Read Mode Command Input
H	L	⎍↑	L	H	X	X	H	Read Mode Address Input
L	H	⎍↑	L	H	X	H	H	Write Mode Command Input
H	L	⎍↑	L	H	X	H	H	Write Mode Address Input
L	L	⎍↑	L	H	L/H	H	H	Data Input
L	L	H	L	↓⎍	L/H	X	H	Sequential Read and Data Output
L	L	H	L	H	L/H	X	L	During Read (Busy)
X	X	X	X	X	L/H	H	L	During Program (Busy)
X	X	X	X	X	X	H	L	During Erase (Busy)
X	X	X	X	X	X	L	X	Write Protect
X	X	X	H	X	0V/V_{CC}	0V/V_{CC}	X	Standby

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
(steady line)	Steady	
(falling hatched)	Changing from H to L	
(rising hatched)	Changing from L to H	
(crosshatched)	Don't Care, Any Change Permitted	Changing, State Unknown
(center line)	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

AC CHARACTERISTICS
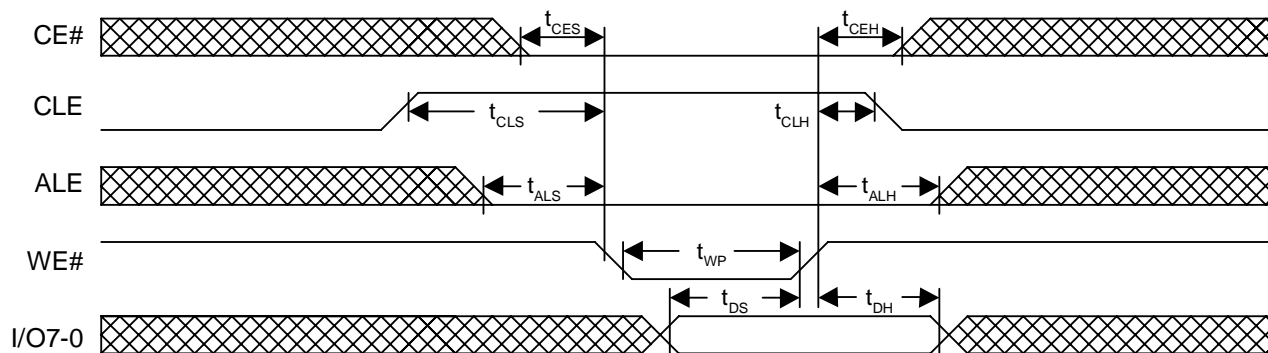
22203A-20

Figure 15.   Command Input Cycle
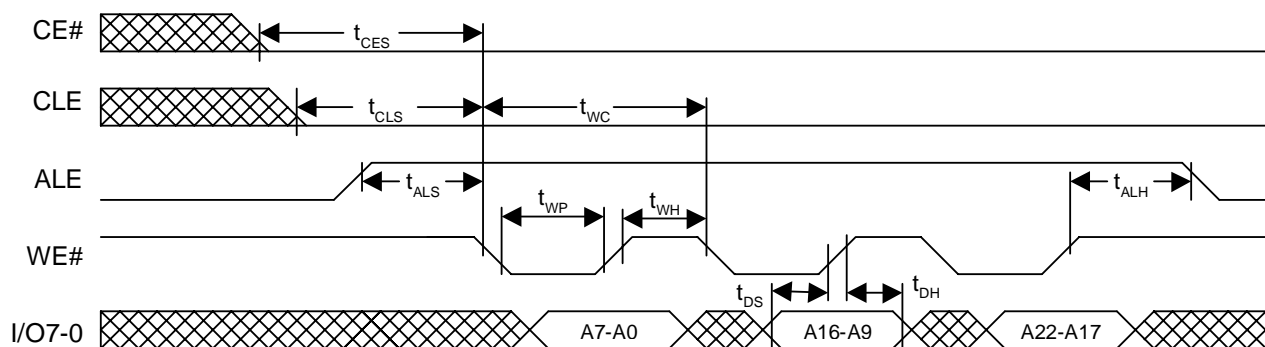
22203A-21

Figure 16.   Address Input Cycle

AMD

AC CHARACTERISTICS
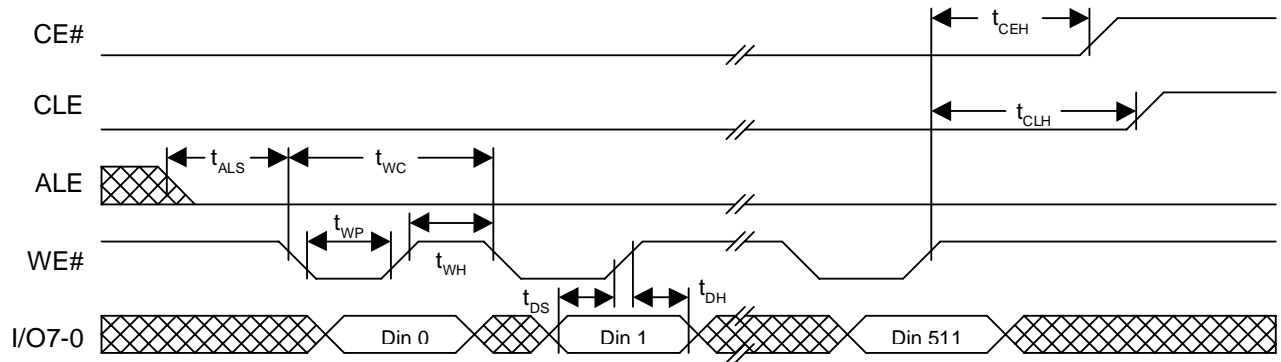
22203A-22

Figure 17.   Data Input Cycle
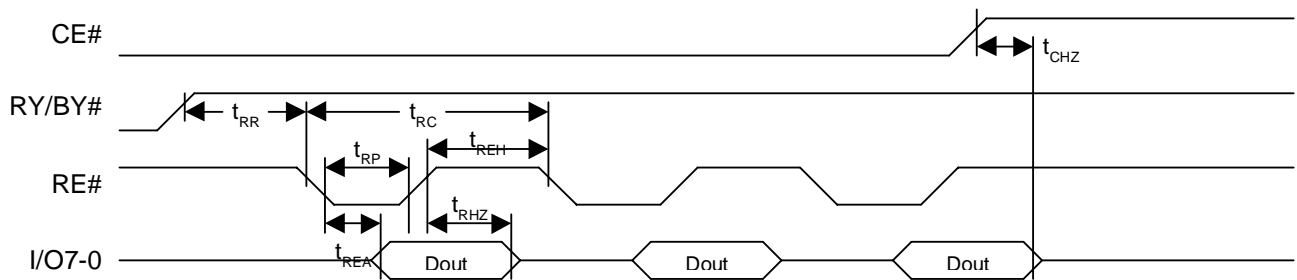
22203A-23

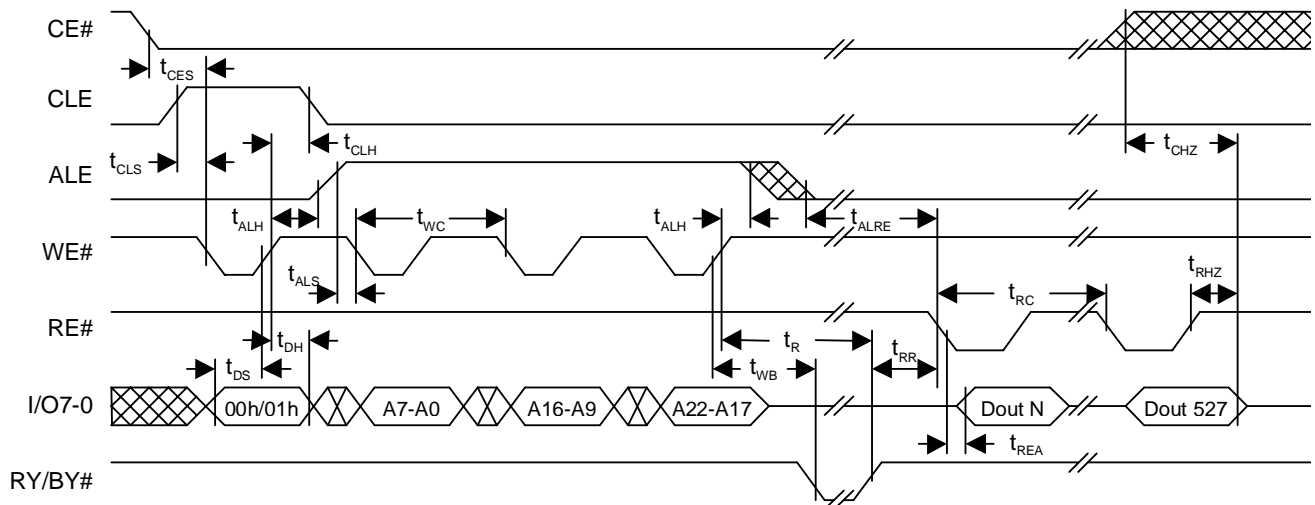**Figure 18.   Serial Read Cycle**
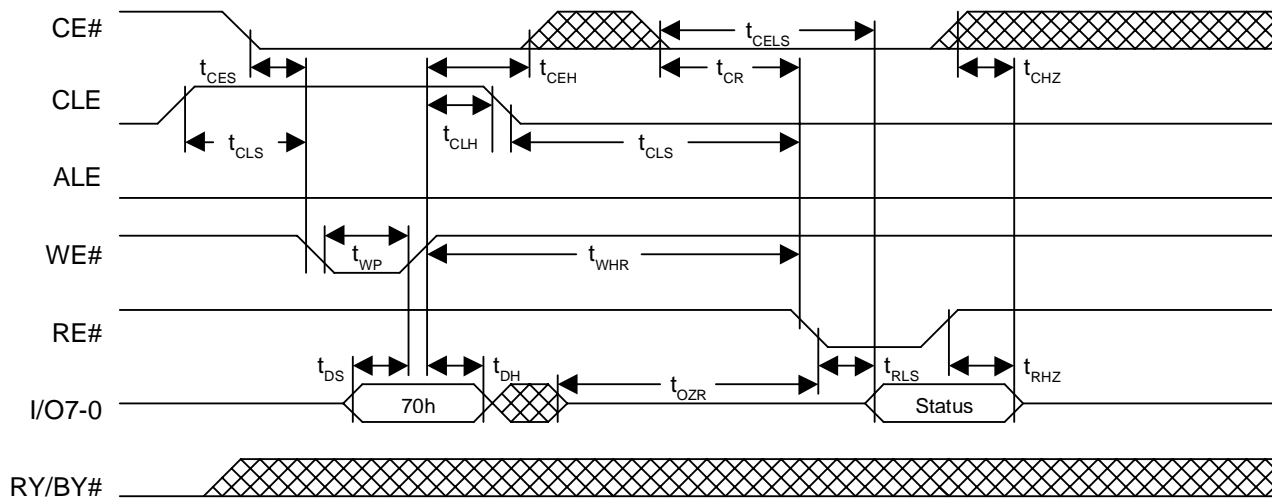
22203A-24

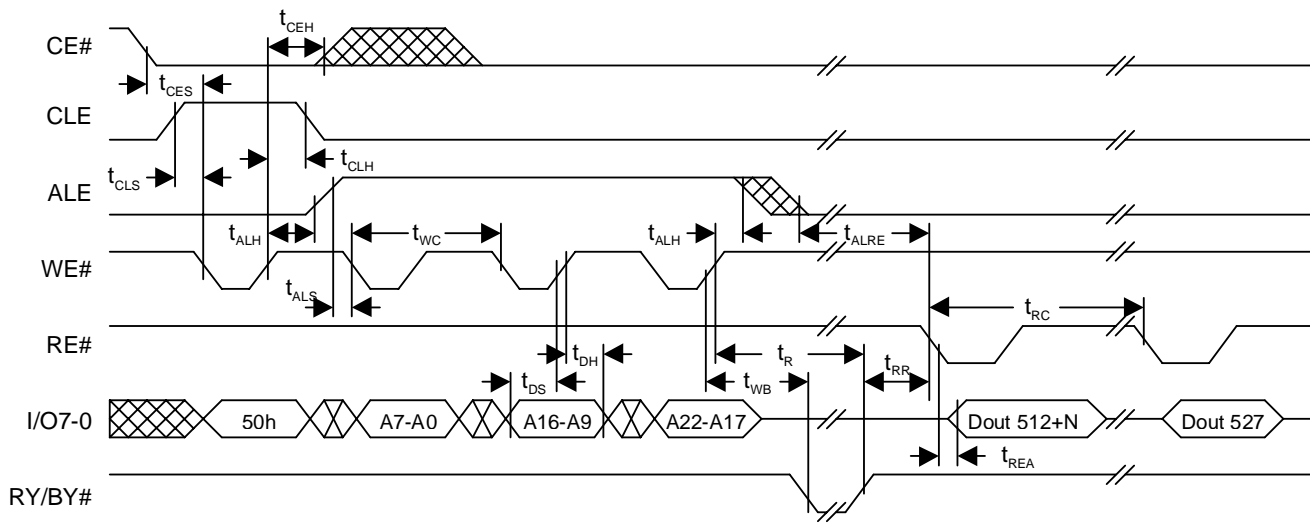**Figure 19.   Status Read Cycle**

AC CHARACTERISTICS
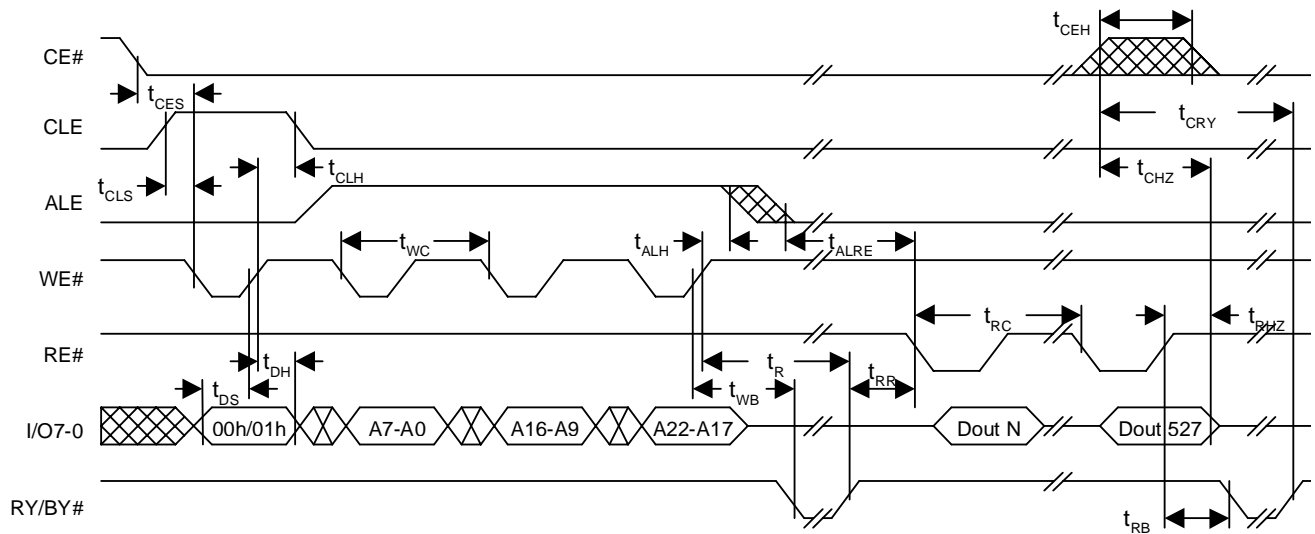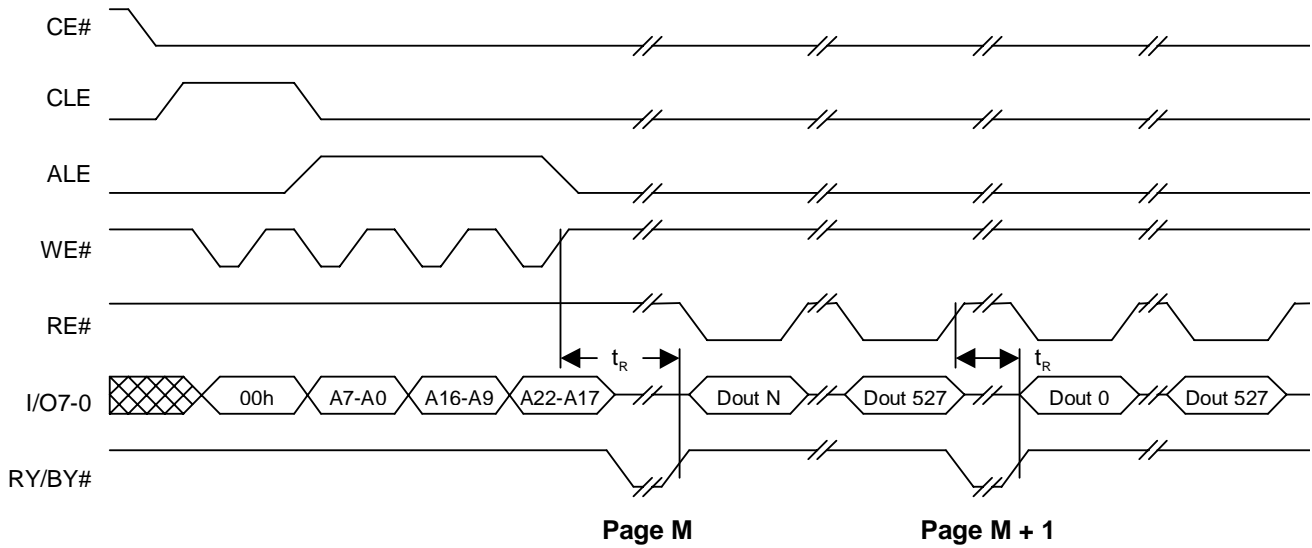

22203A-25

Figure 20.   Read Data

22203A-26

Figure 21.   Read Data (Interrupted by CE#)

AC CHARACTERISTICS

Figure 22.   Read Spare Area

Page M   **Page M + 1**

22203A-28

Figure 23.   Sequential Read

AC CHARACTERISTICS
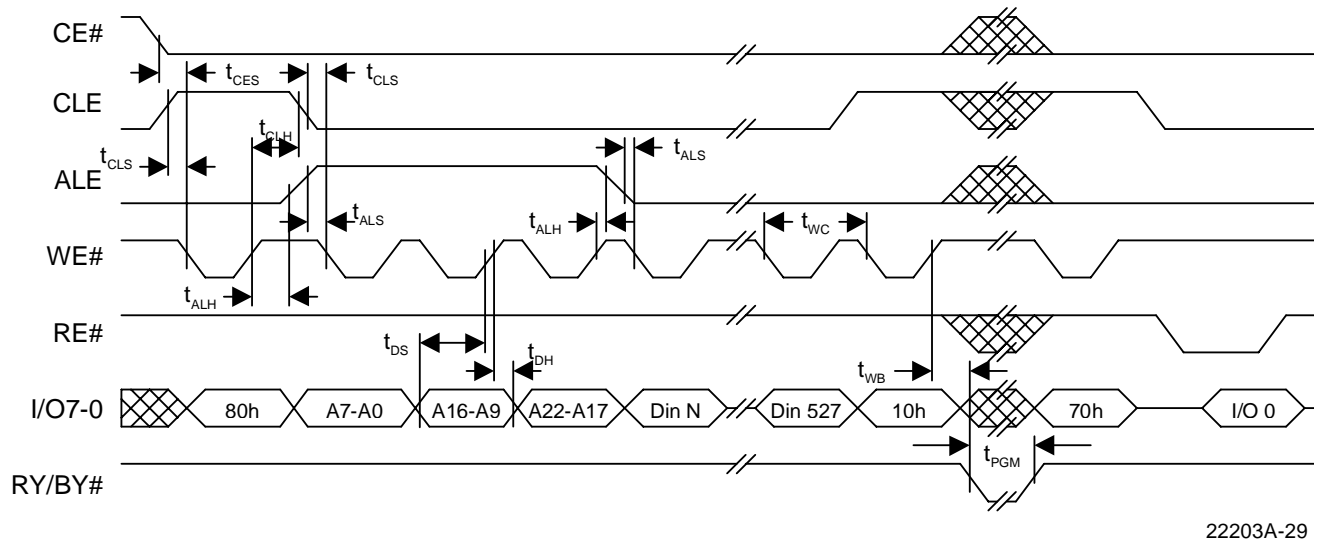
Figure 24.   Page Program
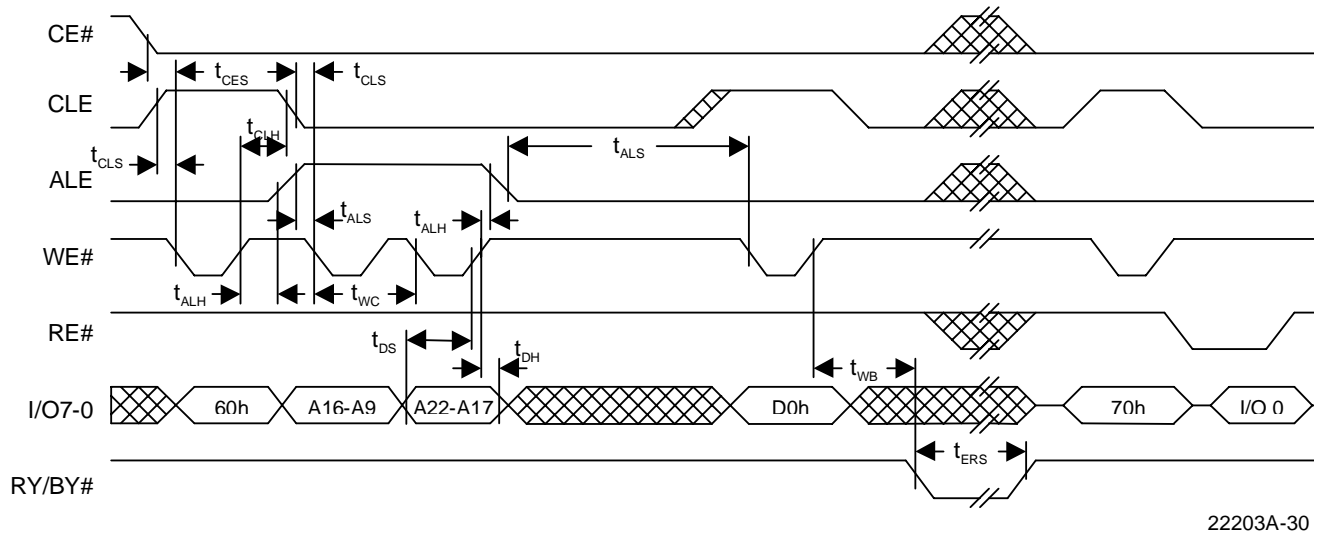
Figure 25.   Block Erase
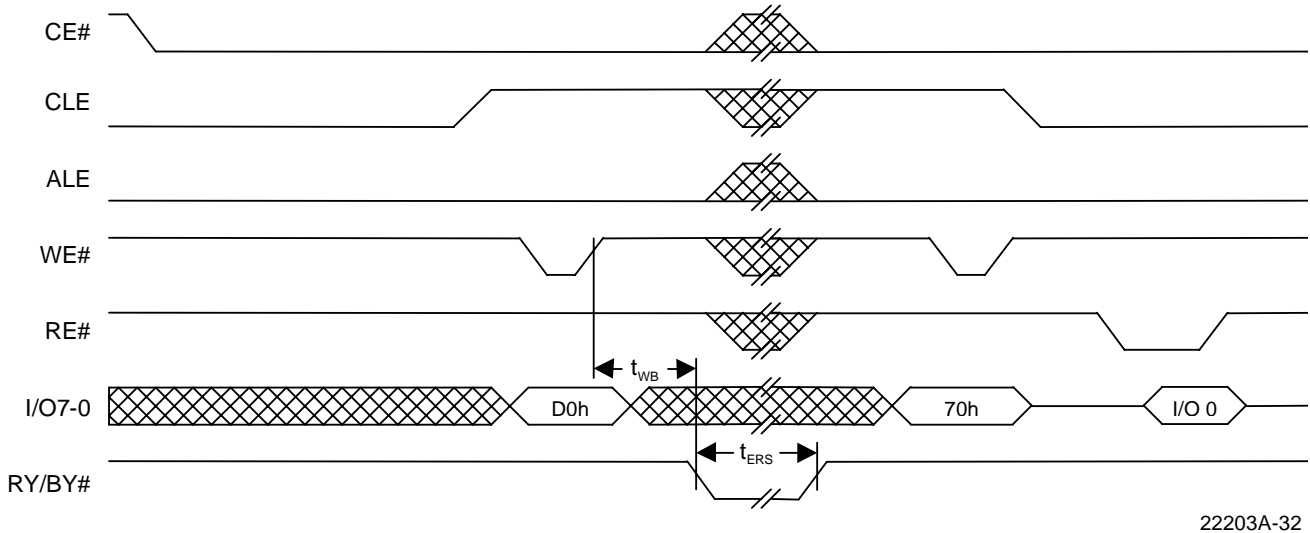
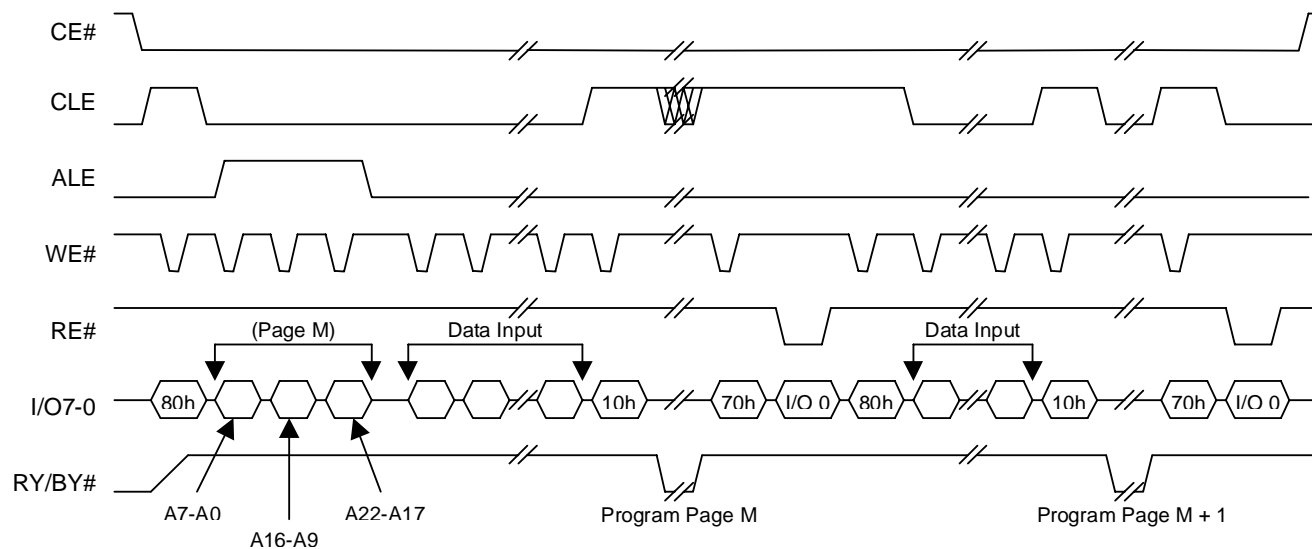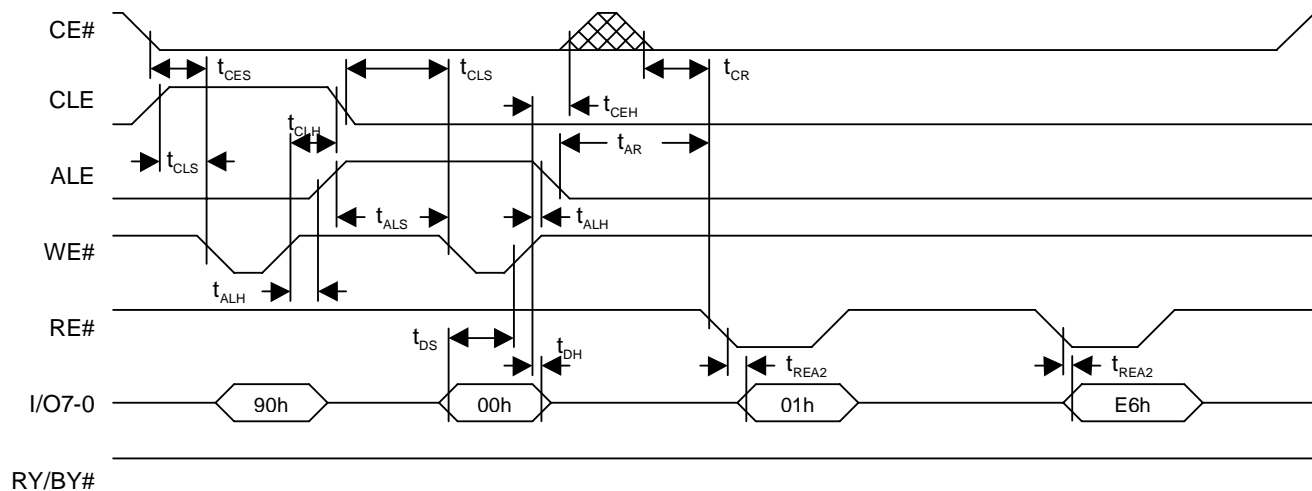## AC CHARACTERISTICS
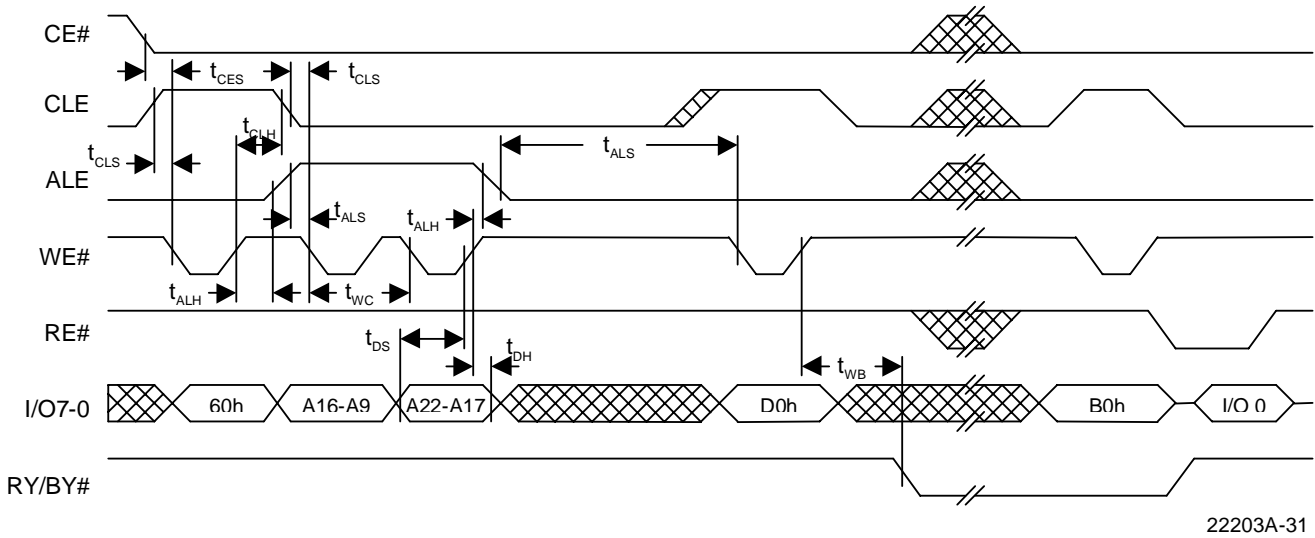
Figure 26. Erase Suspend

Figure 27. Erase Resume

AC CHARACTERISTICS
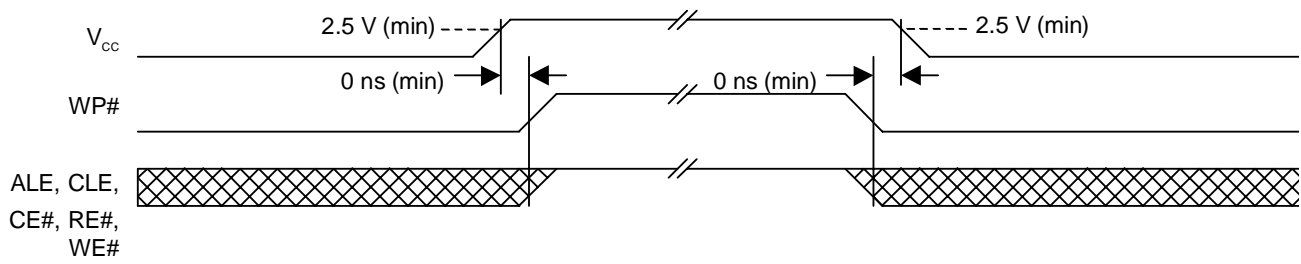

22203A-33

Figure 28.   Sequential Page Program

22203A-34

Figure 29.   ID and Manufacturer Read

AC CHARACTERISTICS

22203A-35

Figure 30.   Write Protect (WP#) Timing During Power Transitions

PROGRAM AND ERASE CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Read Data Transfer Time	–	6.5	7	µs
t_{PGM}	Page Program Time	–	0.2	1.0	ms
t_{ERS}	Block Erase Time	–	2	10	ms

VALID BLOCKS

Symbol	Parameter	Min	Typ	Max	Unit
J40 $N_{V/B}$	Number of Valid Blocks	1024	1024	1024	Blocks
K40 $N_{V/B}$		1014	1020	1024	Blocks

Notes:

1. *The J40 device is guaranteed to ship with all valid blocks (no invalid blocks).*

2. *The K40 device may contain up to 10 invalid blocks which contain one or more invalid bits. The first block is guaranteed to be a valid block. The array of a new device will be completely erased before it is shipped. Some zeros will be programmed into the first and second page of each invalid block. These invalid blocks should be masked out by the system. If a program or erase operation fails on a block over time, it should also be masked out by the system.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP II PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*

2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	85°C	10	Years

AMD

PHYSICAL DIMENSIONS
44/40-Pin Standard Thin Small Outline Package II

TBD

PHYSICAL DIMENSIONS

44/40-Pin Reverse Thin Small Outline Package II

TBD

AMD

PHYSICAL DIMENSIONS
40-Ball Fine Pitch Ball Grid Array

TBD

Trademarks